With reference to Figure 1, there is shown an interposer arrangement, in partial cross-section, fabricated in accordance with the present invention. Interposer 1 is fabricated from a flexible dielectric layer 3 of low modulus material such as, for example, Rogers 2800 material, Dow 1-4173 material or GE 3281 material. Layer 3 may have an elastic modulus in the range of about 50,000 psi to about 400,000 psi. The thickness of flexible dielectric layer 3 may range between 10 to 15 mils. This may be obtained by laminating several layers of Rogers 2800 material, for example, with heat and pressure to form this thickness. An array of vias 5 are formed in the layer, each approximately 2 mils in diameter. These vias may be fabricated by laser ablation, for example. The array of vias are patterned to match the pattern of connection points on the flip chip die and corresponding connection points on the circuit card chip carrier to which it will be interposed and connected. The vias are then copper plated to form copper walls 6. This may be achieved by first plating all of layer 3 with electroless copper. A plating resist is then applied to the vias and both sides of the layer. A mask is aligned to retain resist in the vias and at sites surrounding the end of the vias so as to form top pads 7 and bottom pads 9 at the respective ends of the copper walls. Each pad may be approximately 4 mils in diameter. The resist is then exposed and developed and exposed copper on both sides removed after which the resist is stripped off. Further plating may then be carried out. For some applications, the copper plated vias could then be filled with a conductive adhesive composition, if necessary, but the arrangements shown in Figures 5 and 7 use a different approach.

A1

On page 9, delete the paragraph starting with line 6 and ending with line 21 and replace with:

Figure 6 shows another arrangement for attaching interposer 1 to chip die 23. In this arrangement, flexible dielectric layer 3 described in Figure 1 is first laminated to the bottom of chip die 23 before any vias are formed. This may be done by placing the interposer and chip die in a lamination press and subjecting same, depending on materials, to heat (about 180 - 400°C) and pressure (about 250-2000 psi) for at least 1 hour. Then, the interposer material is laser ablated to form vias through to the underside of chip die 23 to expose BLM pads 27. The assembly is then cleaned to remove any contamination on surfaces inside the holes and on the interposer surface and these surfaces are then subjected to electroless copper plating. It can be seen that here, copper deposits not only on via walls at 15 but also at the bottom of the vias at 16 on BLM pads 27. Unwanted copper is then removed using the process described with respect to Figure 1, leaving copper at the bottom and side walls of the holes and at the interposer surface to form pads 9 around the holes. Thereafter, similar to Figure 5, low melt solder balls 29 are attached to pads 9 on the bottom of interposer 1.

In the Claims:

Please cancel Claim 8.

Please amend Claims 1, 5, 7, 9, 10 and 13 as follows: